FPGA Prototyping of A High Data Rate LTE Uplink Baseband Receiver

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***Abstract*—The Third Generation Partnership Project (3GPP) Long Term Evolution (LTE) standard is becoming the appropriate choice to pave the way for the next generation wireless and cellular standards. While the popular OFDM technique has been adopted and implemented in previous standards and also in the LTE downlink, it suffers from high peak-to-average-power ratio (PAPR). High PAPR requires more sophisticated power amplifiers (PAs) in the handsets and would result in lower efficiency PAs. In order to combat such effects, the LTE uplink choice of transmission is the novel Single Carrier Frequency Division Multiple Access (SC-FDMA) scheme which has lower PAPR due to its inherent signal structure. While reducing the PAPR, the SC-FDMA requires a more complicated detector structure in the base station for multi-antenna and multi-user scenarios. Since the multi-antenna and multi-user scenarios are critical parts of the LTE standard to deliver high performance and data rate, it is important to design novel architectures to ensure high reliability and data rate in the receiver. In this paper, we propose a flexible architecture of a high data rate LTE uplink receiver with multiple receive antennas and implemented a single FPGA prototype of this architecture. The architecture is verified on the WARPLab (a software defined radio platform based on Rice Wireless Open-access Research Platform) and tested in the real over-the-air indoor channel.**

I. Introduction

The uplink transmissions in the 3rd Generation Partnership Project (3GPP) Long Term Evolution (LTE) [1] is based on single carrier frequency division multiple access (SC-FDMA), which is a promising technique for high data rate and low peak-to-average-power ratio (PAPR) in uplink communications in future cellular systems [2], [3]. Multiple-input multiple-output (MIMO) wireless communication systems are capable of providing data transmission at very high data rates and reliability. However, the high data rate and high complexity of LTE uplink receivers complicate the hardware implementation. Hence, the system architecture should be well designed to achieve high data rate and good error-rate performance.

This paper presents an architecture and an FPGA prototype of an LTE uplink MIMO receiver. This work, to the best of the author's knowledge, is the first FPGA prototype of the LTE uplink receiver that integrates several advanced algorithms and features. The rest of the paper is organized as follows: Section II presents the system model. In section III, the algorithm and structure of MIMO detector in LTE uplink receiver system will be given. The architecture of this receiver and the system verification are described in section IV. Section V and VI show FPGA implementation of the proposed architecture and give some brief discussion about system performance and scalability. Finally, we conclude this paper in Section VII.

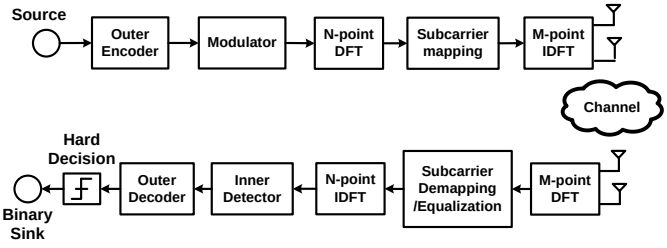

Fig. 1. Linear model of MIMO system in LTE uplink receiver.

II. System Model

Consider a MIMO LTE uplink system with N_t transmit antennas and N_r receive antennas [4]. The vector of information bits is first encoded with an error correcting code and then interleaved to obtain the coded bits. We assume a system with 2^Q-ary modulation with C_h symbols per block per antenna. After modulation, the data sequence is multiplexed into N_t transmission blocks, each containing C_h symbols. Let $d^i_{p,n}(i = 0, \cdots, C_h - 1)$ denote the ith unit-energy symbol in a subsequence transmitted by the nth antenna. Then a DFT transforms the transmission blocks into frequency domain subsequence $\{D^i_{p,n}\}(i = 0, \cdots, C_h - 1)$. Then the coded bits are mapped into subcarriers. Finally, the frequency domain sequence is transformed back to time domain by IDFT before transmission. The overall channel memory is assumed to be N. The received signal vector at the mth sampling time with a block $\mathbf{y}^m$ is given by

$$\mathbf{y}^m = \sum_{n=1}^{N_t} \sum_{i=1}^{N} \mathbf{h}^i_n d^{n-i}_n + \mathbf{n}^m, \tag{1}$$

where $\mathbf{h}^i_n$ is the overall channel impulse response with respect to d^{n-i}_n, and $\mathbf{n}^m$ represents the additive white Gaussian noise vector with zero-mean and variance σ^2. Assume the channel information is perfectly known by the receiver. The received signal sequence is first transformed into the frequency domain by DFT. The frequency domain vector on the mth subcarrier is given by

$$\mathbf{Y}^m = \sum_{n=1}^{N_t} \mathbf{H}_n^m D_n^m + \mathbf{N}^m, \tag{2}$$

where $\mathbf{Y}^m$, $\mathbf{H}_n^m$, D_n^m, and $\mathbf{N}^m$ denote the DFT of $\mathbf{y}^m$, $\mathbf{h}_n^i$, d_n^i, and $\mathbf{n}^m$, respectively.

III. MIMO Detection for LTE Uplink

A. MMSE-FDE

There are three major types of equalizers: time domain equalizers, frequency domain equalizers [5] and combined equalizers [6]. For high ISI channels, time domain equalizers have high complexity and become unattractive to implement. Among frequency domain equalizers (FDE), zero-forcing FDE (ZF-FDE) and minimum mean-square error FDE (MMSE-FDE) equalizers are the simplest ones. The MMSE-FDE equalizer has better performance than the ZF-FDE. Some equalizers belong to the third type. For example, the block MMSE equalizer [2] is a type of equalizer operating in both time and frequency domains. This equalizer can achieve better bit error rate (BER) performance with much higher algorithmic complexity. Because of the simple architecture and relatively good performance, the MMSE-FDE is chosen in our implementation.

MMSE-FDE minimizes the mean square error between its output and the symbols transmitted from the transmitter. The equation for an MMSE-FDE is:

$$\mathbf{Y}' = (\hat{\mathbf{H}}^{\mathrm{H}}\hat{\mathbf{H}} + \sigma^2\mathbf{I})^{-1}\hat{\mathbf{H}}^{\mathrm{H}}\mathbf{Y}, \tag{3}$$

where $\hat{\mathbf{H}}$ is an estimated channel matrix of $\mathbf{H}$ for each subcarrier. $\hat{\mathbf{H}}$ is the output of channel estimation module.

B. MIMO Detection

Maximum likelihood (ML) search is the optimum detection method, which minimizes the BER. This scheme assumes an exhaustive search over the set of all possible transmitted symbol vectors $\mathbf{\Lambda}$ for the minimum square error given by:

$$\hat{\mathbf{s}}_{ML} = \arg\min_{\mathbf{s}\in\Lambda} ||\mathbf{Hs} - \mathbf{y}||^{\mathbf{2}}. \tag{4}$$

However, the complexity of full ML search is too high. Even with modern silicon technology the full ML search is still not feasible, especially for the MIMO detection with multiple antennas and high modulation orders [7].

C. LLR Function for APP Detection

The outer soft decoder calculates the maximum *a posteriori* (MAP) or *a posteriori* probability (APP) values. The soft APP information is exchanged between inner detector and outer decoder, and it is used as additional *a priori* knowledge in the form of a vector of log-likelihood ratio (LLR) values. The magnitude of the LLR value corresponds to the reliability of the decision. The larger the LLR is, the more reliable the decision for a decoded bit is.

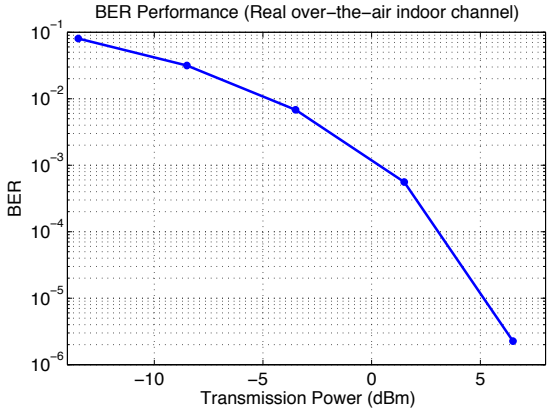

Fig. 2. The BER performance of LTE uplink receiver, 2×2 MIMO, 16-QAM.

Sphere detection (SD) solves the complexity problem of ML detection with some acceptable performance loss. In [8], the authors proposed a computationally efficient SD and list sphere detection (LSD) to achieve near-capacity performance on a MIMO system. The candidates list $\mathfrak{L}$ was used to compute the APP information for each transmitted bit x_k. It is assumed that iterative detection and decoding of bits x that correspond to one channel usage are performed. Then the LLR value of the bit x_k, $k = 0, \cdots, M \cdot M_C - 1$, conditioned on the received vector symbol $\mathbf{y}$ can be expressed as:

$$\begin{aligned} L_E(x_k|\mathbf{y}) \approx & \frac{1}{2}\max_{x\in\mathfrak{L}|\mathbf{X}_{k,+1}} \left\{-\frac{1}{\sigma^2}\|\mathbf{y} - \mathbf{H}\cdot\mathbf{s}\|^2 + x_{[k]\cdot\mathbf{L}_{A,[k]}}^T\right\} \\ & -\frac{1}{2}\max_{x\in\mathfrak{L}|\mathbf{X}_{k,-1}} \left\{-\frac{1}{\sigma^2}\|\mathbf{y} - \mathbf{H}\cdot\mathbf{s}\|^2 + x_{[k]\cdot\mathbf{L}_{A,[k]}}^T\right\}, \end{aligned} \tag{5}$$

where M is the number of transmit antennas, and M_C is the number of bits per constellation symbol.

Based on (5), we designed an APP unit to calculate the APP information used by the inner detector and outer decoder with reduced hardware complexity. This APP unit is reconfigurable and can be used in different soft MIMO detectors.

Notice that in (5), $-\frac{1}{\sigma^2}\|\mathbf{y} - \mathbf{H}\cdot\mathbf{s}\|^2$ has been calculated as a partial Euclidean distance (PED) in sphere detector. Therefore, the APP unit can take full advantage of the soft information from the inner detector to reduce the complexity of the hardware system.

D. Simulation Results

The 2×2 MIMO receiver is verified on the Rice WARPLab platform [9]. WARPLab is a scalable and extensible programmable wireless platform based on software radio to prototype advanced wireless networks. Signals generated in MATLAB can be transmitted in real-time over the air using WARP nodes. This facilitates rapid prototyping of Physical layer algorithms. The goal of this simulation is to verify that our receiver system satisfies the system requirements of the LTE standard.

Fig. 2 shows the BER performance for 2×2 MIMO receiver, where 16-QAM modulation is used. The length of DFT and IDFT are 128 and 72, respectively. The length of codeword

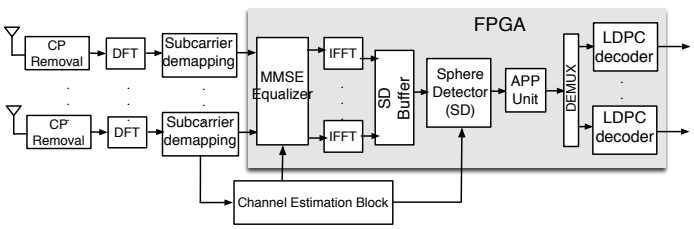

Fig. 3. The system diagram of LTE uplink receiver. This system is 2×2 MIMO system.

TABLE I
PARAMETERS FOR A 2×2 MIMO LTE UPLINK RECEIVER

Parameter	Description
Channel bandwidth	1.4MHz∼20MHz
Modulation order	QPSK, 16-QAM, 64-QAM
Number of symbols (per antenna)	72∼1200
Number of subcarriers (per antenna)	128∼2048
Coding	LDPC code, rate=1/2 length=576bits∼2304bits
Equalizer	MMSE-FDE

for LDPC decoder is 576. This system is tested in a real over-the-air indoor channel to verify the algorithm performance.

IV. ARCHITECTURE

A. Overall Architecture of LTE Uplink Receiver

As can be seen in Fig. 3, a physical layer prototype system for the LTE uplink receiver is designed, including IDFT, MMSE-FDE, sphere detector [10], APP unit and LDPC decoder [11]. Table I shows the implementation parameters in detail.

B. MMSE-FDE

If the MMSE-FDE is directly built using (3), we need a large wordlength to achieve a good precision. This is because the range of values of $\hat{\mathbf{H}}^{\mathrm{H}}\hat{\mathbf{H}} + \sigma^{\mathbf{2}}\mathbf{I}$ is much larger than the original $\hat{\mathbf{H}}$. Researchers use different approaches to solve this problem. In [12], the authors use more bits to perform the matrix inversion than other operations to guarantee no overflow in inversion. In [13], blockwise matrix inversion is used to break a large inversion into a few small inversions. In [14], the authors use a modified Gram-Schmidt QR decomposition with a dynamic scaling algorithm which enhances numerical stability. All of the above approaches are based on either inverting the matrix $\hat{\mathbf{H}}^{\mathrm{H}}\hat{\mathbf{H}} + \sigma^{\mathbf{2}}\mathbf{I}$ [12] [13], or performing the QR decomposition on an extended matrix, which is larger than $\hat{\mathbf{H}}$ [14]. In order to further minimize the area and increase the speed, here we propose a new method. Equation (3) is converted into the following form:

$$(\hat{\mathbf{H}}^{\mathrm{H}}\hat{\mathbf{H}} + \sigma^{\mathbf{2}}\mathbf{I})^{-\mathbf{1}}\hat{\mathbf{H}}^{\mathrm{H}}\mathbf{Y} = (\hat{\mathbf{H}} + \sigma^{\mathbf{2}}(\hat{\mathbf{H}}^{\mathrm{H}})^{-\mathbf{1}})^{-\mathbf{1}}\mathbf{Y}. \quad (6)$$

Compared with (3), equation (6) only needs to invert $\hat{\mathbf{H}}$ which has a much smaller range of values. This corresponds to a small wordlength during inversion. Also when $\sigma^{\mathbf{2}}$ goes to zero, the equalizer will not become unstable. Because (6) will converge to $(\hat{\mathbf{H}})^{-\mathbf{1}}$, the MMSE-FDE will gradually converge to a less accurate ZF-FDE. Another simplification is to reduce the number of multipliers in complex multiplication by using strength reduction.

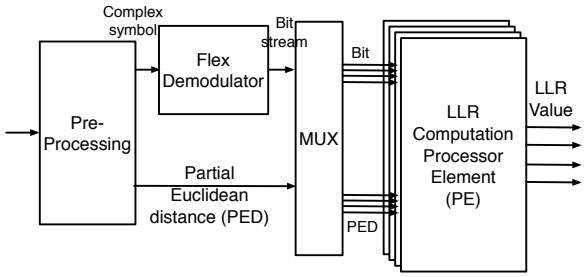

Fig. 4. The top level diagram of the architecture of APP unit. The soft SD in this architecture is Flex SD.

C. APP Function Unit

APP unit without feedback loop can be implementation based on (5). The inputs to the APP unit are the output candidates from the sphere detector. We use a flex sphere detector (SD) in our implementation [10] since it can handle different modulations and antenna configurations with low overhead.

The Flex SD receives the equalized symbols from the MMSE-FDE, and produces a list of candidates per each channel usage; this means in a 2×2 MIMO system, Flex SD will produce candidates for 2 MIMO symbols per clock cycle. For a 16-QAM scenario, the Flex SD outputs 8 candidates in every cycle, and in 8 continuous clock cycles, it will generate 64 candidates in all for 2 transmitted MIMO symbols [10]. Each candidate contains 2 MIMO symbols and a partial Euclidean distance (PED) value.

Fig. 4 shows the top level architecture of the APP unit. The main parts include the preprocessing module, flexible n-QAM demodulator, multiplexing module, and several LLR computation processor elements (PE). The preprocessing module retrieves PED values and two complex symbols from the input. Then the complex symbols are demodulated through the flexible n-QAM demodulator that can support QPSK, 16-QAM and 64-QAM. PEs calculate the LLR value for each coded bit using demodulated bits and the corresponding PED values. A fully parallel architecture is utilized, that is, in order to process all $M \cdot M_C$ bits of two symbols in parallel, we need $M \cdot M_C$ PEs working simultaneously.

There are several changes in the interface between detector and decoder to enable the iteration loop to achieve extra performance improvement. Fig. 5 shows the architecture of APP unit with a feedback loop.

V. FPGA IMPLEMENTATION

We implemented most of the block units in the system of Fig. 3 using Xilinx System Generator. The system is designed for 2×2 MIMO receiver for the LTE uplink in which 2048

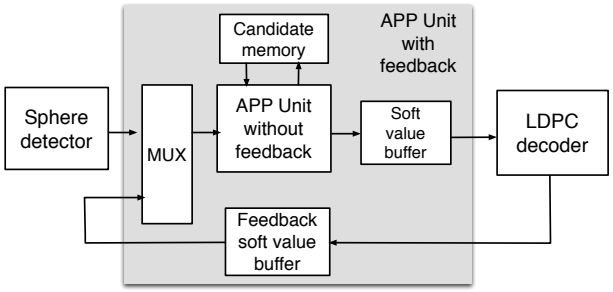

Fig. 5. The architecture of the APP unit with iterative loop. Two buffers, one candidate memory and a multiplexing have been added.

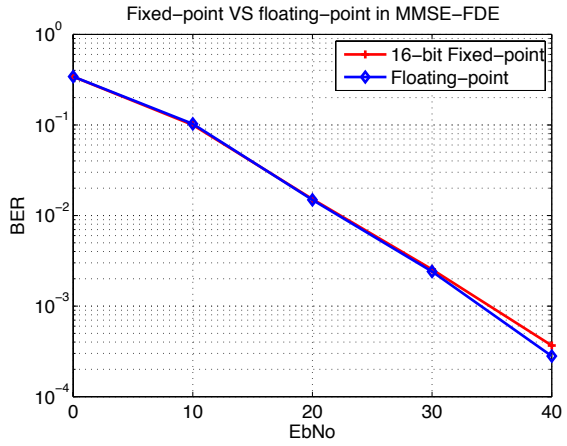

Fig. 6. Performance comparison between fixed-point implementation and floating-point for MMSE-FDE block.

subcarriers are transmitted and 1200 subcarriers are occupied by symbols. 16-QAM and 2304-bit LDPC code are used. It is noticeable that since the system is reconfigurable, we could easily change the parameters of the receiver so that it could support other profiles in the LTE standard.

A. MMSE-FDE

The performance comparison between fixed-point implementation and floating-point is shown in Fig. 6. Before 30dB, the two curves are almost the same. The performance loss after 30dB occurs since σ^2 becomes zero and the MMSE-FDE reduces to the less accurate ZF-FDE as mentioned in Section IV.

Xilinx System Generator is used to implement the proposed MMSE-FDE. Table II shows the Xilinx ISE synthesis results of the FPGA implementation.

TABLE II
FPGA RESOURCE UTILIZATION SUMMARY OF THE PROPOSED MMSE-FDE FOR THE XILINX VIRTEX-4, XC4VFX100-10FF1517 DEVICE

Number of Slices	5,145/42,176 (12%)
Number of 4 input LUTs	9,019/84,352 (10%)
Number of DSP48s	64/160 (40%)
Max. Frequency	99.461MHz
Max. Data Rate	397.844Mbps

B. APP Function Unit

We use Xilinx System Generator to implement the proposed APP unit architecture. The APP unit processes the input data in parallel, and can be extended to support higher modulation orders and more antennas. By replacing multiplications with shift and addition operations, we reduce the number of multipliers required and get higher maximum frequency. Table III shows the Xilinx ISE synthesis result of the APP function unit.

TABLE III
FPGA RESOURCE UTILIZATION SUMMARY OF THE PROPOSED APP UNIT FOR THE XILINX VIRTEX-4, XC4VFX100-10FF1517 DEVICE

Number of Slices	2,393 /42,176 (5%)
Number of 4 input LUTs	4,426 /84,352 (5%)
Number of DSP48s	0 /160 (0%)
Max. Frequency	208MHz
Max. Data Rate	1.628Gbps

C. Other Block Units

Table IV and Table V show the FPGA implementation results for sphere detector and LDPC decoder blocks, respectively. All of these parts are reconfigurable. We use the Xilinx DFT core [15] to perform DFT and IDFT operations in our system.

TABLE IV
FPGA RESOURCE UTILIZATION SUMMARY OF IDFT BLOCK FOR THE XILINX VIRTEX-4

Number of Slices	3,748 /42,176 (8%)
Number of 4 input LUTs	5,699 /84,352 (6%)
Number of DSP48s	16 /160 (10%)
Max. Frequency	234MHz
Max. Data Rate	936Mbps

TABLE V
FPGA RESOURCE UTILIZATION SUMMARY OF SPHERE DETECTOR BLOCK FOR THE XILINX VIRTEX-4, XC4VFX100-10FF1517 DEVICE

Number of Slices	7,780 /42,176 (18%)
Number of 4 input LUTs	14,300/84,352 (16%)
Number of DSP48s	81 /160 (50%)
Max. Frequency	220MHz
Max. Data Rate	220Mbps

VI. SYSTEM PERFORMANCE AND IMPLEMENTATION CONSIDERATIONS

A. System Performance

In our LTE uplink receiver system, the parameters are set as below: 2 receiving antennas, 2048 subcarriers, 1200 occupied subcarriers, 16-QAM, 2304-bit LDPC for 20MHz channel bandwidth. By using two clock domains, with MMSE-FDE, IDFT, APP unit and LDPC decoder in one slower clock domain, and sphere detector in the other faster clock domain, the current system can achieve a data rate of up to 220Mbps.

This data rate is much higher than the requirement given by LTE standard, which is 115.2Mbps for 20MHz channel bandwidth under the 2×2 16-QAM scenario [1].

B. Higher Data Rate

LTE standard specifies signal transmissions in six possible channel bandwidths ranging from 1.4MHz to 20MHz [1], [3]. There are 72 occupied subcarriers available in a 1.4MHz channel and 1200 occupied subcarriers available in a 20MHz channel. The data rate of a 20MHz channel for a 2×2 64-QAM uplink system is 172Mbps. To support this configuration, the overall architecture of our system does not need to change. We only need to configure the sphere detector and APP unit to 64-QAM mode. Accordingly, because the size of the transmission signal sequence becomes larger, we should increase the size of the buffer between blocks.

C. System Scalability

During implementing, in order to simplify the design process, we assume that the input data comes from one user. However, we could extend our receiver to support multi-user access. As is depicted in Fig. 3, most of the blocks do not need to change except for a few modifications. The first difference is, instead of using an N-point IDFT block, we should replicate a few IDFT blocks with small length, each of which is for one user. Another modification is to add LDPC decoders for multiple users. In order to separate the codeword for each user, a de-multiplexing is required between the APP computation unit and LDPC decoder. It is noticeable that by replicating blocks for different users, we do not modify the overall architecture or redesign the function unit blocks. More hardware resources and more chip area are required when extending the system by replicating function blocks. However, there are opportunities to reduce the usage of hardware resources. For example, we could exploit the potential reuse of the IDFT blocks and it is probable that some blocks could share specific hardware resources.

VII. Conclusion and Future Work

This paper proposed a flexible architecture of the high data rate LTE uplink receiver, which integrates several advanced algorithms and features. A single FPGA prototype of this architecture is presented. It supports different numbers of antennas and modulation orders. The prototype is implemented using Xilinx System Generator and is verified on the WARPLab platform with channels generated by the Azimuth channel emulator. We also verified the system in real over-the-air indoor channels.

The FPGA prototype we built can be fit in one Xilinx Virtex4 FX140 FPGA. It supports data rates up to 220Mbps, which is much higher than the data rate requirement of the LTE standard. The prototype of our LTE uplink receiver can be configured to support different transmission bandwidths specified by the LTE standard.

The future work is to extend our LTE uplink receiver to support multi-access from different users. We will further optimize the whole system to reduce the usage of hardware resources by balancing the resource usage among different parts of the system. For example, we could reuse some modules and match the rates of different modules. Furthermore, with this platform, we will investigate more complicated algorithms with potentially better performance, such as the block MMSE equalizer and more sophisticated iterative detection-decoding schemes. We will also try to increase the reconfigurability of the receiver in order that it can be configured on the fly.

Acknowledgments

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