Guohui Wang

Curriculum Vitae

Department of Electrical and Computer Engineering
Rice University, Houston, TX 77005
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Research Interests

Mobile computing, GPGPU parallel computing, VLSI design, wireless communication.

Education

2008–present **Ph.D candidate, Electrical Engineering**, *Rice University*, *Houston, TX*, (GPA: 4.11/4).

2005–2008 **M.S., Computer Science**, *Chinese Academy of Sciences*, *Beijing, China*.

2001–2005 **B.S., Electrical Engineering**, *Peking University*, *Beijing, China*.

B.S., Economics, *Peking University*, *Beijing, China*.

Work Experience

2014–present **Senior System Engineer**, *Qualcomm*, *San Diego, CA*.
Study and analyze GPGPU compute solutions for mobile processors.

2012 Summer **Intern**, *Qualcomm*, *San Diego, CA*.
(Received Qualstar Diamond Award)
Research on CPU-GPU heterogeneous computing on mobile SoC processors.

2011 Summer **Intern**, *National Instruments R&D*, *Austin, TX*.
Design and implementation of 1Gbps 8x8 MIMO LTE-Advanced transceiver prototype.

Research Experience

2008–present **Research Assistant**, *Rice University*, *Houston, TX*.

- **CPU-GPU heterogeneous computing for mobile systems using OpenGL ES and OpenCL programming models.** *(Related publications: JSPS'2014a, GlobalSIP'2013a, ICASSP'2013a, ICASSP'2013b)*
- **GPGPU accelerators for high performance DSP algorithms such as error-correction codes and MIMO detection for wireless communication systems.** *(Related publications: JSPS'2014b, GlobalSIP'2013b, ASILOMAR'2013, GTC'2013, ASILOMAR'2012, SASP'2011, ASILOMAR'2011, JSPS'2011)*
- **Parallel and configurable VLSI architecture and implementation of data detection and error-correction codes for high performance communication systems.** *(Related publications: TCAS-I, ICASSP'2014a, ICASSP'2014b, ASAP'2013, ISCAS'2013, ASILOMAR'2012, ASAP'2011, ISCAS'2011, ASILOMAR'2009)*
- **Design and implementation of DSP accelerators using High-Level Synthesis (HLS) tools.** *(Related publications: ASILOMAR'2009)*

2005–2008 **Research Assistant**, *Chinese Academy of Sciences*, *Beijing, China*.

- **VLSI architecture and FPGA implementation for HD cinema decoding system.**
  Designed and implemented FPGA-based SoC architecture for high throughput image decoding subsystem for the DCI-complaint 2K High-definition digital cinema systems.

Publications

Book chapter

Y. Sun, **G. Wang**, B. Yin, J. R. Cavallaro and T. Ly, "High-level Design Tools for Complex DSP Applications", *DSP for Embedded and Real-Time Systems: Expert Guide*, Elsevier, 2012. ISBN-13: 9780123865359.

Talks

"Massively Parallel Signal Processing for Wireless Communication Systems", technical lecture on *GPU Technology Conference (GTC-2013)*. March 18-21, 2013, San Jose, California.

Journal papers

G. Wang, H. Shen, Y. Sun, J. R. Cavallaro, A. Vosoughi, and Y. Guo, "Parallel Interleaver Design for a High Throughput HSPA+/LTE Multi-Standard Turbo Decoder", *IEEE Transactions on Circuits and Systems-I: Regular Papers (TCAS-I)*. (Invited. Accepted for publication)

G. Wang, Y. Xiong, J. Yun, and J. R. Cavallaro, "Computer Vision Accelerators for Mobile Systems based on OpenCL GPGPU Co-Processing", submitted to *Journal of Signal Processing Systems (JSPS)*. (Invited. Accepted for publication)

M. Wu, B. Yin, **G. Wang**, C. Dick, J. R. Cavallaro, and C. Studer, "Large-Scale MIMO Detection for 3GPP LTE: Algorithm and FPGA Implementation", submitted to *IEEE Journal of Selected Topics in Signal Processing (JSTSP)*. (Accepted for publication)

M. Wu, B. Yin, **G. Wang**, C. Studer, and J. R. Cavallaro, "GPU Acceleration of a Configurable N-Way MIMO Detector for Wireless Systems", submitted to *Journal of Signal Processing Systems (JSPS)*, 2013. (Invited. Accepted for publication)

M. Wu, Y. Sun, **G. Wang**, and J. R. Cavallaro, "Implementation of a High Throughput 3GPP Turbo Decoder on GPU", *Journal of Signal Processing Systems (JSPS)*, 2011.

Y. Sun, **G. Wang**, and J. R. Cavallaro, "Parallel VLSI Architecture for 3GPP LTE/LTE-Advanced Turbo Decoder", submitted to *IEEE Transaction on Signal Processing (TSP)*. (Under review)

G. Wang, Z. Zhu, K. Zhang, and Z. Wang, "A Novel Design Of the High Speed Buffer and Video/audio Synchronization in High Resolution Digital Cinema System", *High Technology Letters (In Chinese)*, Vol.9, 2008.

Conference papers

G. Wang, B. Yin, I. Cho, J. R. Cavallaro, S. Bhattacharyy, and J. Takala, "Efficient Architecture Mapping of FFT/IFFT for Cognitive Radio Networks", to appear at *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP)*, 2014.

B. Yin, M. Wu, **G. Wang**, C. Dick, J. R. Cavallaro, and C. Studer, "A 3.8 Gb/s Large-scale MIMO Detector for 3GPP LTE-Advanced", to appear at *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP)*, 2014.

G. Wang, M. Wu, and J. R. Cavallaro, "High Throughput Low Latency LDPC Decoding on GPU for SDR Systems", *1st IEEE Global Conference on Signal and Information Processing (GlobalSIP)*, 2013. (invited)

G. Wang, B. Rister, and J. R. Cavallaro, "Workload Analysis and Efficient OpenCL-based Implementation of SIFT Algorithm on a Smartphone", *1st IEEE Global Conference on Signal and Information Processing (GlobalSIP)*, 2013.

M. Wu, **G. Wang**, B. Yin, C. Studer, and J. R. Cavallaro, "HSPA+/LTE-A Turbo Decoder on GPU and Multicore CPU", *47th Asilomar Conference on Signals, Systems, and Computers (ASILOMAR)*, 2013. (invited)

A. Vosoughi, **G. Wang**, H. Shen, J. R. Cavallaro, and Y. Guo, "Highly Scalable On-the-Fly Interleaved Address Generation for UMTS/HSPA+ Parallel Turbo Decoder", *24th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, 2013.

G. Wang, Y. Xiong, J. Yun, and J. R. Cavallaro, "Accelerating Computer Vision Algorithms Using OpenCL Framework on the Mobile GPU - A Case Study", *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP)*, 2013.

B. Rister, **G. Wang**, M. Wu, and J. R. Cavallaro, "A Fast and Efficient SIFT Detector using the Mobile GPU ", *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP)*, 2013.

G. Wang, A. Vosoughi, H. Shen, J. R. Cavallaro, and Y. Guo, "Parallel Interleaver Architecture with New Scheduling Scheme for High Throughput Configurable Turbo Decoder", *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2013. **(Finalist, best student paper award)**.

G. Wang, H. Shen, B. Yin, Y. Sun, and J. R. Cavallaro, "Parallel Nonbinary LDPC Decoding on GPU", *46th Asilomar Conference on Signals, Systems, and Computers (ASILOMAR)*, 2012.

B. Yin, M. Wu, **G. Wang**, and J. R. Cavallaro, "Low Complexity Opportunistic Decoder for Network Coding", *46th Asilomar Conference on Signals, Systems, and Computers (ASILOMAR)*, 2012.

G. Wang, M. Wu, Y. Sun, and J. R. Cavallaro, "GPGPU Accelerated Scalable Parallel Decoding of LDPC Codes", *45th Asilomar Conference on Signals, Systems, and Computers (ASILOMAR)*, 2011.

G. Wang, Y. Sun, J. R. Cavallaro, and Y. Guo, "High-Throughput Contention-Free Concurrent Interleaver Architecture for Multi-Standard Turbo Decoder", *IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, 2011.

G. Wang, M. Wu, Y. Sun, and J. R. Cavallaro, "A Massively Parallel Implementation of QC-LDPC Decoder on GPU", *IEEE Symposium on Application Specific Processor (SASP)*, 2011.

Y. Sun, **G. Wang**, and J. R. Cavallaro, "Multi-Layer Parallel Decoding Algorithm and VLSI Architecture for Quasi-Cyclic LDPC Codes", *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2011.

G. Wang, B. Yin, K. Amiri, Y. Sun, M. Wu, and J. R. Cavallaro, "FPGA Prototyping of A High Data Rate LTE Uplink Baseband Receiver", *43rd Asilomar Conference on Signals, Systems and Computers (ASILOMAR)*, 2009.

Posters

"Parallel Interleaver Design for High Throughput Configurable Turbo Decoder", *Annual Rice University ECE Affiliates Day Conference*, March 2013. **2nd place winner best graduate student poster**.

"Parallel Interleaver Design for High Throughput Configurable Turbo Decoder", *IEEE Texas Workshop on Integrated System Exploration (TexasWISE)*, March 2013.

"Low Energy Fast SIFT Detector on Heterogeneous Mobile Processors", *IEEE Texas Workshop on Integrated System Exploration (TexasWISE)*, March 2013.

Patents

G. Wang, A. Vosoughi, H. Shen, J. R. Cavallaro, and Y. Guo, "System and method for parallel interleaver for high data rate turbo decoder". U.S. Patent Application. Filed in July, 2012.

G. Wang, Y. Sun, J. R. Cavallaro, and Y. Guo, "System and Method for Contention-Free Memory Access". U.S. Patent U.S. Patent US8621160 B2. Filed by Huawei, December 2011. Granted, December 2013. (Also published as CN103262425A, WO2012079543A1)

A. Vosoughi, **G. Wang**, H. Shen, J. R. Cavallaro, and Y. Guo, "Scalable interleaved address generation for UMTS/HSPA+ turbo decoder". U.S. Patent Application. Filed in July, 2012.

G. Wang, Z. Wang, Z. Wei, Z. Zhu, "The Method, System and Device to Implementing Video/audio Synchronization", China Patent ZL200710120585.0. Filed in August, 2007; granted in September, 2012.

G. Wang, Z. Wei, Z. Wang, "A Fast and High Performance Method for Multimedia Video Zooming", China Patent ZL200710178188.9. Filed in 2007. Granted in October, 2011.

Z. Wei, Z. Wang, **G. Wang** "A method of Watermark Generation and Detection for digital cinema Copyright Protection", China Patent ZL200810103472.4. Filed in 2008. Granted in September, 2010.

Z. Zhu, Z. Wang, X. Wang, Z. Wei, **G. Wang**, "A copyright protection method and system for audio and video contents in digital cinema", China Patent ZL200810114749.3. Filed in 2008. Granted in March, 2010.

Honors and Awards

2013 **Best student paper award nominee**, IEEE International Symposium on Circuits and Systems (ISCAS).

2013 **Second place winner of best poster contest**, Annual Rice ECE Affiliates Conference.

2012 **Student travel grant**, ACM/IEEE International Symposium on Computer Architecture (ISCA).

2008 **Graduate student fellowship**, Department of ECE, Rice University.

Teaching Experience

2009–2012 **Course lab instructor**, *ECE Department, Rice University*.
ELEC 220: Fundamental of Computer Engineering
Teach lab sessions, prepare and conduct weekly three-hour lectures reviewing the week's course material and explaining lab project materials, grade homework and projects.

2010 **Teaching assistant**, *ECE Department, Rice University*.
ELEC 522: Advanced VLSI Design

2009 **Teaching assistant**, *ECE Department, Rice University*.
ELEC 303: Random Signals

Academic Services

Reviewer for journals

IEEE Journal of solid State Circuits (JSSC), IEEE Transactions on Signal Processing (TSP), IEEE Transactions on Parallel and Distributed Systems (TPDS), IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I), IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II), IEEE Transactions on Circuits and Systems for Video Technology (TCSVT), IEEE Transactions on Very Large Scale Integration Systems (TVLSI), IEEE Transactions on Multimedia (TMM), IEEE Transactions on Aerospace and Electronic Systems (TAES), IEEE Transactions on Service Computing (TSC), IEEE Communications Letters (CL), IEEE Computer Architecture Letters (CAL), ACM Transactions on Embedded Computing Systems (TECS), Journal of Parallel and Distributed Computing (JPDC), Journal of Computer Science and Technology (JCST), EURASIP Journal on Wireless Communications and Networking (JWCN), Frontiers of Computer Science (FCS), Circuits, Systems and Signal Processing (CSSP), Signal, Image and Video Processing (SIVP), Concurrency and Computation: Practice and Experience (CPE), Parallel Computing (PARCO).

Reviewer for international conferences

IEEE International Symposium on Circuits and Systems (ISCAS), IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP), IEEE Clobal Communication Conference (GLOBECOM), IEEE Global Conference on Signal and Information Processing (GlobalSIP), European Signal Processing Conference (EUSIPCO), IEEE International Conference on Communications (ICC), ACM Great Lakes Symposium on VLSI (GLSVLSI), IEEE Workshop on Signal Processing Systems (SiPS), International Symposium on Information Theory and its Applications (ISITA), IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), IEEE International Wireless Communications and Mobile Computing Conference (IWCMC), IEEE Symposium on Industrial Electronics & Applications (ISIEA).

Activities

2009–2012 Committee member of **Rice Center for Engineering Leadership (RCEL)**.

2009–2012 Graduate Student Mentor Program in ECE Department, Rice University.

References

Available upon request.

Publications